REMARKS/ARGUMENTS

1.) Claim Amendments

The Applicant has amended claim 16; no new subject matter has been added. Claims 13-24 remain pending in the application.

2.) Examiner Objections – Specification

The Examiner objected to the abstract of the disclosure because it was not submitted on a separate sheet in accordance with 37 C.F.R. §1.52(b)(4). Although the application is a national stage application filed under 35 U.S.C. §371, which is not subject to the requirements of §1.52(b)(4), the Applicant submits herewith a copy of the abstract on a separate sheet.

3.) Claim Rejections – 35 U.S.C. §112, 2nd ¶

The Examiner rejected claim 16 as being indefinite. The Applicant has amended claim 16 to correct a typographical error, changing its dependency from claim 13 to claim 15, which corrects the lack of antecedent basis for the term "said channels."

4.) Claim Rejections – 35 U.S.C. §102(e)

The Examiner rejected claims 13-24 as being anticipated by Paneth, *et al.* (U.S. Patent No. 6,393,002). The Applicant traverses the rejections.

It is important to remember that anticipation requires that the disclosure of a single piece of prior art reveals every element, or limitation, of a claimed invention. Furthermore, the limitation that must be met by an anticipatory reference are those set forth in each statement of function in a claims limitation, and such a limitation cannot be met by an element in a reference that performs a different function, even though it may be part of a device embodying the same general overall concept. Paneth fails to disclose each and every limitation of claims 13-24 and, therefore, those claims are not anticipated thereby.

Claim 13 recites:

> 13. A Processing Unit (PA) for processing a plurality of data streams by an algorithm divided into a plurality of process steps, said PA comprising:
>
> an interconnection unit comprising means for switching;
>
> Process Step (PS) means comprising at least two PS modules, where each PS module is connected to the interconnection unit and a scheduler connected to said interconnection unit and to each PS module;:
>
> a memory unit comprising at least two memories wherein each memory is connected to the interconnection unit;
>
> the interconnection unit further comprising means for providing at least a first connection between one of said memories and one of said PS modules and a second connection between another of said memories and another of said PS modules, wherein the interconnection unit is adapted to connect each memory to each of the PS modules by a switching activity, wherein the switching activity and the processing of the PS modules are controlled by the scheduler; and
>
> each memory comprises means for storing a data stream and said stored data streams are manipulated in parallel by the connected PS modules respectively, during a predetermined time period between said switching activities. (emphasis added)

The Applicant's invention is directed to a processing unit architecture for processing a plurality of data streams by an algorithm divided into a plurality of process steps. The processing unit includes at least two process step modules, each of which are connected to an interconnection unit and a scheduler. The interconnection unit is further connected to at least two memory modules. The interconnection unit includes means for connecting each of the memory modules to each of the process step units under the control of the scheduler. Each of the memory units can store a data stream and the stored data streams are manipulated in parallel by the connected process step modules, respectively, during a predetermined time period. Paneth fails to disclose those claim limitations.

In asserting that Paneth teaches the claim limitations, the Examiner points to Figure 5 and column 5, lines 5-58, as disclosing the claimed process step modules. Although Figure 5 is stated by Paneth to illustrate "various data processing modules,"

there is no teaching therein that the process modules are coupled to an interconnection unit for selectively-coupled to different memory units under the control of a switching activity. Furthermore, column 5, lines 5-58, merely discloses a Glossary of Acronyms used in the specification.

With respect to the claim limitation of "memory units [that] can [each] store a data stream and the stored data streams are manipulated in parallel by the connected process step modules, respectively, during a predetermined time period," the Examiner points to column 7, lines 24-59, and column 28, line 65 to column 29, line 60, stating that Paneth discloses "a database module is utilized to store and transmit data streams according to the scheduler that can utilize timer events." Even if Paneth discloses storing and transmitting data streams according to a scheduler that can utilize timer events, that is not equivalent to multiple memory units that can each store a data stream, and wherein the data streams are manipulated in parallel by process step modules coupled to the multiple memory units by an interconnection unit.

For at least the foregoing reasons, Paneth fails to teach all of the limitations of claim 13; therefore, claim 13 is not anticipated. Whereas independent claim 19 recites limitations analogous to those of claim 13, it is also not anticipated by Paneth. Furthermore, whereas claims 14-18 and 20-24 are dependent from claims 13 and 19, respectively, and include the limitations of their respective base claims, those claims are also not anticipated by Paneth.

* * *

CONCLUSION

In view of the foregoing amendment and remarks, the Applicant believes all of the claims currently pending in the Application to be in a condition for allowance. The Applicant, therefore, respectfully requests that the Examiner withdraw all rejections and issue a Notice of Allowance for claims 13-24.

The Applicant requests a telephonic interview if the Examiner has any questions or requires any additional information that would further or expedite the prosecution of the Application.

Respectfully submitted,

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